

***High Speed Counter
Model 621-0307RC
User Manual***

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**USER MANUAL CROSS REFERENCE
FOR MODEL 621-0307RC HIGH SPEED COUNTER**

MANUAL:	MATERIAL COVERED:
High Speed Counter Model 621-0307RC User Manual Form No. 621-8992	Counter Operating Modes; Input Operation; Output Operation; Installation; Wiring and Programming.
621 I/O Specifications User Manual Form No. 620-8995	I/O system overview; Detailed Module Descrip- tions (digital input, digital output, special func- tion); Serial I/O system; Fuse and battery re- quirements.
620-10 and 620-15 Processor User Manual Form No. 620-8999	Detailed Hardware Description; 620-10 and 620- 15 System Configurations (processor and I/O); Modes of Operation; Processor Diagnostics; Instruction Sets and Opcodes.
620-20 Processor User Manual Form No. 620-8998	Detailed Hardware Description; 620-20 System Configuration (processor and I/O); Modes of Operation; Processor Diagnostics; Instruction Set and Opcodes.
620-25 and 620-35 Processor User Manual Form No. 620-8984	Detailed Hardware Description; 620-25 and 620-35 System Configurations (processor and I/O); Modes of Operation; Processor Diagnostics; Instruction Set and Opcodes.
620 Installation User Manual Form No. 620-8996	620 System Overview; System Configuration for all processor models, parallel and serial I/O; Address- ing; Rack Assembly Mounting; Module Settings (jumpers and DIP switches); Module Installation; Cable and Conduit Routing; Wiring; Reference Information on Superseded Model Numbers.

INTRODUCTION

The 621-0307RC High Speed Counter I/O Module allows 620-15, 620-20, 620-25, 620-30, or 620-35 controller systems to count high speed pulse streams, primarily from quadrature-type incremental shaft encoders. Other devices providing a pulsed output may also be used.

The HSC module occupies two I/O card slots in either the 621 I/O rack or the 620-15 processor rack I/O section. The HSC module cannot be installed within the 620-20 or 620-25 processor I/O rack slots. It accepts pulses from one encoder with either a 5V TTL or a differential output. The HSC contains two user program 16-bit counters that respond to a single pulse input device. These 16-bit counters can be preset. Each counter has an associated 5-15VDC output that either turns on or off when the preset is reached. Each 16-bit counter is controlled separately by the control program. External control inputs provide external count reset and count latch functions for each counter. Counter accumulated values may be read by the user program. The count range is 0 to 65,535 counts, however, overflow and underflow status bits can be used to extend this count range.

MODULE SPECIFICATIONS

CE MARK (Europe) — Conformity with 73/23/EEC, the Low Voltage Directive, and 89/23/EEC, the EMC Directive.

SIGNAL INPUTS-CHANNELS A, B, C - TTL OPERATION

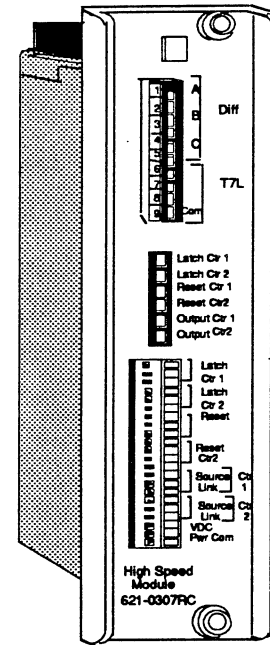
(TTL Inputs A, B, and C are TTL compatible, incorporating a 1.3K pull up resistor to 5VDC.)

Differential Operation

Input Range (max.)	0.5VDC - 12VDC
Common Mode Voltage	±12VDC
Max. Differential Input Voltage	25VDC
Input Sensitivity	±200mV
Hysteresis	±50mV
Maximum Input Frequency	100KHz, unfiltered 200Hz, filtered
Minimum Pulse Width	3usec, unfiltered
Signal Input Isolation	none

CONTROL INPUTS - RESET AND LATCH COUNTER

Input Voltage	5 - 15VDC ±10%
Turn On Voltage	4.5VDC
Turn Off Voltage	1.5VDC
Input Current	5mA min. 34mA max. 7.5mA typ. at 5VDC 24mA typ. at 12VDC
Input Delay	
OFF to ON	2.4ms ±25%



ON to OFF	17.5ms ±25%
Input Isolation	2500VDC optical

COUNTER OUTPUTS

Number per Module	2
Output Voltage	5 - 15VDC
Output Current	150mA Source or Sink

(External Supression Diode required for Inductive Loads)

Output Delay

OFF to ON	15usec max.
ON to OFF	350usec max.

(Measured with max. resistive load from Vcc to 10% of Vcc)

Output Isolation	2500VDC optical
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GENERAL SPECIFICATIONS

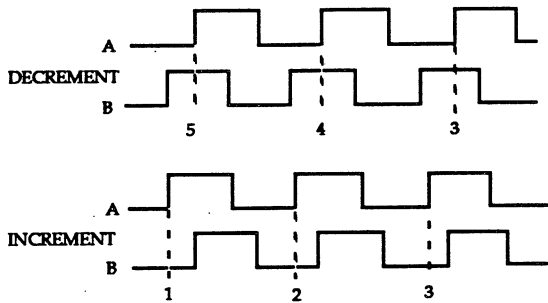
Number of Count Inputs	1 quadrature encoder
620 System Power	
Unit Load	1 amp +5VDC
External Power Supply Requirements	
Control Inputs and Counter Outputs	Inputs and outputs will operate over a 5 - 15VDC range from external power source
Number of counters per module	2
Maximum Preset Value	65535
Temperature	0-60°C
Humidity	5 - 95% non-condensing

COUNTER OPERATING MODES

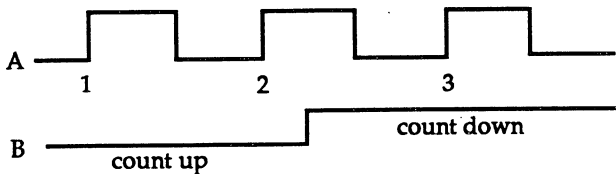
The HSC may be selected for one of four counting modes of operation. They are:

1. Quadrature Input
2. Separate Count with Direction Control
3. Separate Up/Down Count Input
4. Programmable Output Dwell Function

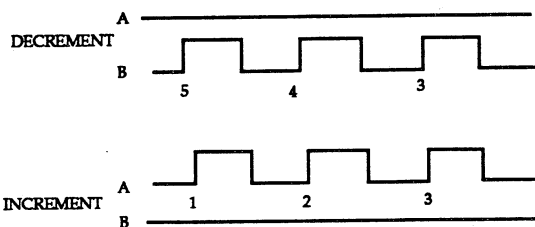
Quadrature Input: The A and B channels determine count direction. When the A pulse leads the B pulse, the counters increment. When a B pulse leads an A pulse, the counters decrement. The normal Quadrature Mode increments or decrements the counters on the rising edge of the A pulse. The quadrature mode may be selected for increased resolution by either counting A and B pulses (X2 operation) or A and B rising and falling edges (X4 operation). The X2 and X4 operation is permissible with quadrature operation only.



Separate Count with Direction Control: This mode permits channel A to accept pulsed inputs while a signal level applied to channel B determines counter direction. Channel B, in its high state (+5VDC), will cause counters to decrement. A low state will cause counters to increment.



Separate Up/Down Count Input: This mode permits Channel A pulses to increment the counters. Channel B pulses decrement the counters.

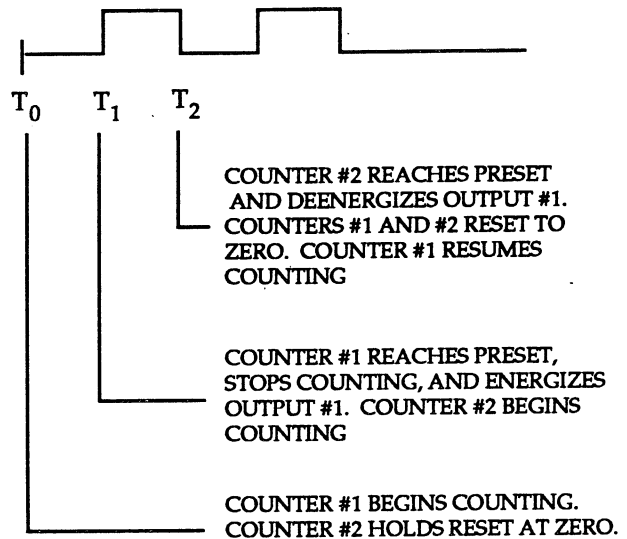


Programmable Output Dwell Function: This special operating mode allows the HSC to provide a modulated pulsed output. The two counters contained on the HSC determine the output pulse width and dwell between pulses as a function of the HSC input pulses.

In this mode, Counter #1 determines the dwell period for Output #1. When the preset value for Counter #1 is reached, Output #1 is energized. At this instant, Counter #1 stops counting and Counter #2 starts counting.

Counter #2 determines the amount of time that Output #1 will remain energized. When Counter #2 reaches its preset value, Output #1 is de-energized. At this instant, Counters #1 and #2 are reset and Counter #1 resumes counting.

COUNTER #1
OUTPUT



Output #2 will automatically assume the opposite state of Output #1 when the dwell function is selected.

INPUT OPERATION

High Speed Counter inputs are divided into two groups: pulse source inputs and external counter control inputs.

The pulse source inputs are located on the top field wiring connector. The HSC may be selected via a DIP switch for pulse inputs from a device providing either a TTL or differential output. There are three pulse inputs; the A Channel input, the B Channel input, and the C Channel input (marker input). A and B Channel inputs cause the two 16-bit counters to operate as described in the COUNTER OPERATING

MODE section. The marker input is used in conjunction with the external counter reset control inputs. The marker signal, provided by most shaft encoders once every revolution, must be in the high state when the external counter reset inputs are energized, before the counters are set to zero.

The pulse source inputs can accurately follow a square wave input at a 50% duty cycle up to a 100KHz rate. These inputs may be filtered via a DIP switch to reduce the input frequency to no greater than 200Hz at 50% duty cycle.

The pulse source inputs when operated in the differential mode utilize SN74175 differential line receivers. This device has the following specifications:

Common Mode Voltage:±12VDC
Max Differential Input Voltage:..... ±25VDC
Input Sensitivity:±200mV
Input Hysteresis:±50mV

Counter control inputs provide external control of the HSC 16-bit counters. There are two reset counter inputs and two latch counter inputs, for control of both 16-bit counters.

When both the reset input and the marker input for a given counter are in the high state, the respective counter is reset to zero. The count will resume when the reset input is turned off. The latch input will cause its respective counter to stop counting when the latch input transitions from a low to a high state. Once the counter receives an external latch command, the latch may be reset through the user program by means of one of the following:

1. a clear latch control output command (counter not reset)
2. a reset counter control output command
3. the external reset counter input

The counter will resume counting when the clear latch control output is turned on, or when the reset control output or external counter reset input is turned off.

The reset counter and latch counter inputs have a 5 - 15VDC operating range. The turn on voltage level is 4.5VDC. The turn off voltage level is 1.5VDC. Electrically isolated from each other, these inputs are filtered and have the following input delay times:

OFF to ON: 2.4ms±25%
ON to OFF: 17.5ms ±25%.

The reset counter and latch counter inputs each have a STATUS LED that illuminates when the respective input is in the high state. The latch counter STATUS LED indicates that input state, not the latch condition (i.e. the latch input may be off, but the counter may still be latched).

OUTPUT OPERATION

The HSC contains two solid state outputs, each responding to its respective 16-bit counter. The outputs are DIP switch selectable to turn on or off when the preset value of each counter is reached. These outputs may also be forced on or off by the user control program.

Each output can be configured for either sink or source operation. See the INSTALLATION section for proper jumper settings with sink/source operation. Each output has an associated status LED that illuminates when the output is energized.

INSTALLATION

CAUTION

Follow these instructions carefully. Failure to follow installation instructions could result in damage to the module.

The HSC may be installed in any two adjacent I/O slots in the 621 I/O rack or the 620-15 processor I/O section. The HSC cannot be installed in the 620-20 or 620-25 processor rack.

CAUTION

This module must not be installed while power is applied to the rack power supply.

The HSC requires the selection of various switch combinations and placement of jumpers in order to obtain the required operation. All switches and jumpers are located on the control board which is the left pcb when viewing the HSC front panel. Remove the component side cover to access switches and jumpers. See Figure 1 for component placement.

The Rotary Selector Switch (S1), a 9-position switch selects the various counting functions. Position 9 selects both the quadrature X1 operating mode and separate count and direction control mode. Positions 8 and 4 select the quadrature X2 and X4 modes respectively. Position 6 selects the separate counts mode of operation. Refer to Table 1.

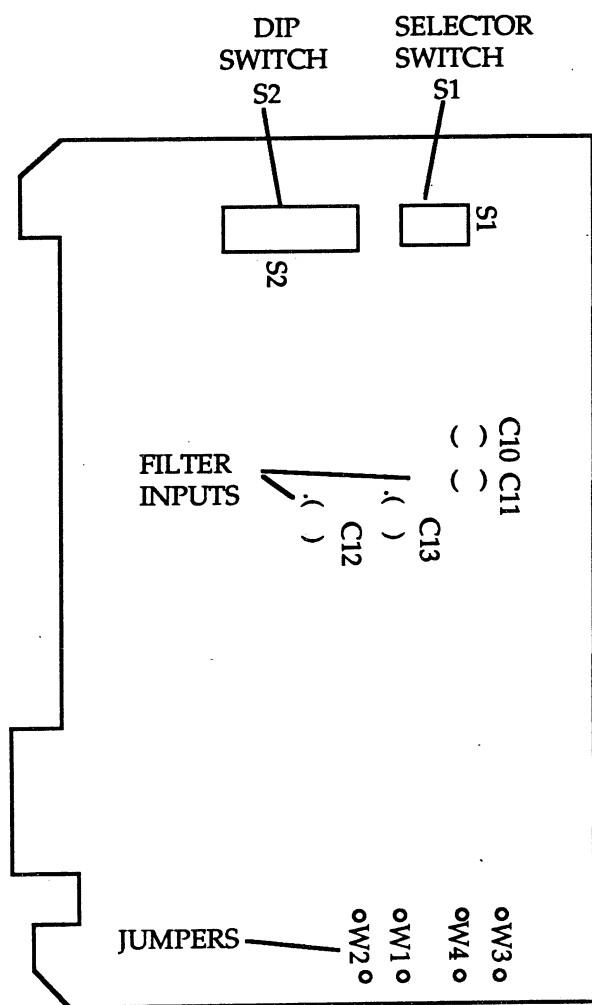


TABLE 1 - S1 SELECTOR SWITCH SETTINGS

POSITION	FUNCTION
0 - 3	Not Used
4	Quadrature X4
5	Not Used
6	Separate Counts
7	Not Used
8	Quadrature X2
9 *	Quadrature X1 and separate count with direction control

* Factory Setting

The eight-position DIP switch (S2) enables/disables pulse input filtering for channels A, B, and C, as well as selects those channels to operate with either TTL or differential output devices. Additionally, this switch enables the programmable output dwell function and determines the state of the module outputs while counting. See Table 2 for S2 DIP switch settings.

FIGURE 1 - HSC COMPONENT PLACEMENT

TABLE 2 - S2 DIP SWITCH SETTINGS

**FACTORY
SETTING:
ALL DIP
SWITCHES
OFF**

POSITION	FUNCTION
1	ON: Channel A filter selected for frequency up to 200Hz OFF: Channel A filter removed for frequency up to 100KHz
2	ON: Channel B filter selected for frequency up to 200Hz OFF: Channel B filter removed for frequency up to 100KHz
3	ON: Channel C filter selected for frequency up to 200Hz OFF: Channel C filter removed for frequency up to 100KHz
4	ON: Select TTL pulse source inputs OFF: Select differential source inputs
5	ON: Dwell function selected OFF: Dwell function disabled
6	ON: Output #1 is on when accumulated count is less than preset OFF: Output #1 is on when accumulated count is greater than/equal to preset
7	ON: Output #2 is on when accumulated count is less than preset OFF: Output #2 is on when accumulated count is greater than or equal to preset
8	Not Used

Jumper positions W1, W2, W3, and W4 are used to select the HSC external outputs for sink or source operation. Two jumpers supplied on the module are used for this purpose. Figure 1 illustrates jumper locations; the following table shows correct jumper placement combinations.

OUTPUT	SOURCE	SINK
Output #1	W1*	W2
Output #2	W3*	W4

* Factory Setting

CAUTION

Make certain that the two jumpers are properly positioned prior to applying power to the outputs. Incorrect placement will result in module damage.

The HSC outputs may drive up to four TTL loads per output by installing the jumpers in W1 or W3 for each output driving TTL devices. In addition, a 68 ohm 1/2 watt pull-down resistor (customer -supplied) must be installed in W2 or W4 for each output that is driving a TTL device.

External latch count and reset inputs are filtered to reduce the effect of contact bounce from mechanical switch closures. Input time delays can be substantially reduced by removing a capacitor from each circuit. This reduces the circuit time delays to the following:

OFF to ON Delay: 130usec ± 20% at 5V
100usec ± 20% at 15V

ON to OFF Delay: 900usec ± 20% at 5V
900usec ± 20% at 15V

Refer to Figure 1 for capacitor location. The following table lists the input each capacitor is associated with.

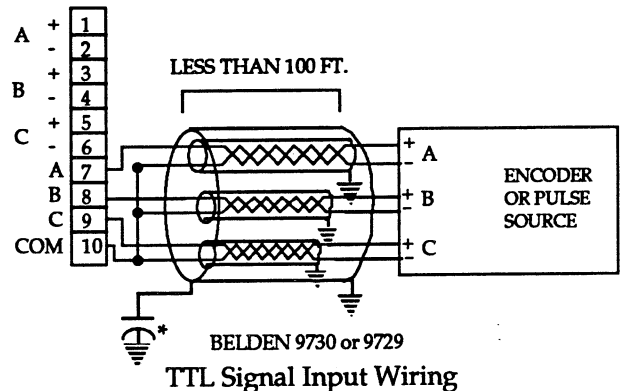
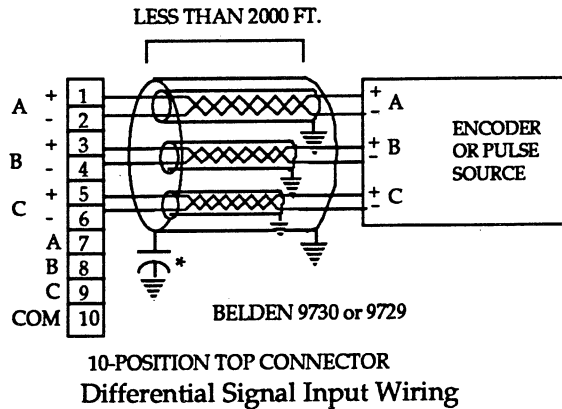
Latch Counter #1:	C10
Latch Counter #2:	C11
Reset Counter #1:	C12
Reset Counter #2:	C13

The HSC requires 1A of 5VDC power supplied by the rack power supply. Make certain that the power supply output is not overloaded. Refer to the 620 SYSTEM INSTALLATION MANUAL (Form 620-8996) for unit load figures.

WIRING

Two connectors are mounted on the HSC. These connectors are two-piece constructions for input and output terminations. The male half may be removed to facilitate wiring and for easy module installation and removal.

All pulse source inputs are wired to the 10-position top connector. See Figure 2 for typical differential or TTL wiring.



* To comply with CE Mark the shields must be connected to the rack chassis ground through a .01 µf capacitor. The rating of the capacitor must be 250 VAC/1.4K VDC.

NOTE: The encoder and HSC chassis grounds must be at the same potential.

FIGURE 2 - TYPICAL SIGNAL INPUT WIRING (A, B, & C CHANNELS)

For pulse source inputs the voltage is provided by the pulse source. TTL pulse source inputs, however, may also be activated by switching the inputs to ground through a contact closure as these inputs are pulled high by internal pull-up resistors.

Pulse Source Input Cabling: Pulse source devices should be connected to the HSC using shielded cable. Cable shields must be grounded at the pulse source.

Belden No. 9730 and 9729 are three and two-twisted pair cables suitable for long distance differential operation (less than 2000 cable feet). TTL operation should be limited to distances less than 100 feet, due to electrical noise present in most applications which may affect pulse signal quality.

External Counter Control Input Cabling: The external counter control inputs (reset and latch for each counter) are wired to terminals 1 through 8 on the lower 14 position connector. Each input is isolated from one another. See Figure 3 for wiring details.

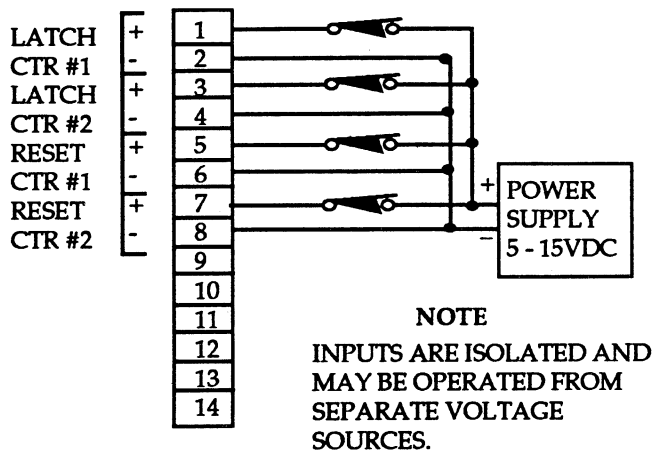


FIGURE 3 - CONTROL INPUT WIRING

External counter control input devices should be connected to the HSC using a twisted shield pair cable (Belden Model No. 8761 or equivalent). Ground the cable shield at the signal source. Avoid running input wiring with high voltage wiring (115VAC or above).

Output Cabling: HSC outputs are wired to terminals 9 through 14 on the lower connector. Each output is selected for either sink or source operation by jumper placement on the module. Figure 4 shows wiring for HSC outputs in either current sinking or sourcing configurations.

CAUTION

HSC outputs are not fuse protected. Make certain that connections are correct before applying power. Diode suppression is required for inductive loads. Use Littelfuse type 3AG CAT No. 312.250 or equivalent. Use diode 1N4001.

PROGRAMMING

The HSC uses the PUSH instruction to send counter preset values to the HSC. The PULL instruction is used to read counter accumulated

TYPICAL COUNTER OUTPUTS

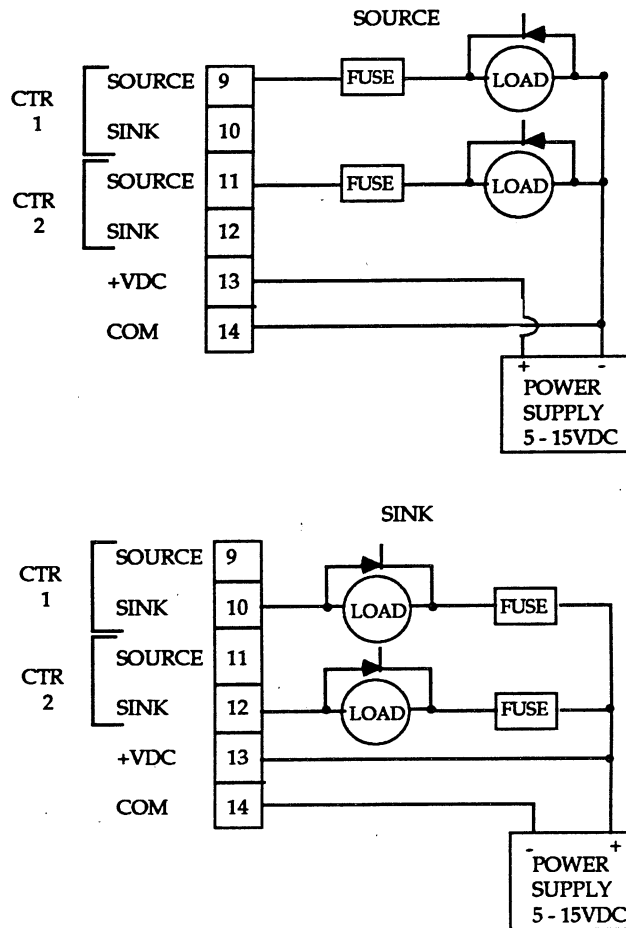


FIGURE 4 - OUTPUT WIRING

values and HSC status bit information. PUSH and PULL instructions are "immediate" instructions (e.g. when a PULL instruction is executed by the 620 processor, it retrieves the specified data from the module at that instant. Likewise, the PUSH instruction sends data to the module at the time it is executed in the control program).

The HSC also responds to output instructions from the processor: -(), -(R), -(L), -(U). These instructions are "immediate" instructions as well and are used for the HSC control functions.

The following section explains PUSH, PULL and Output functions. See Figure 5.

ADDRESSING

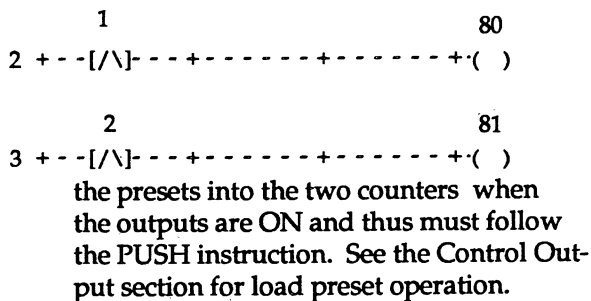
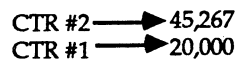
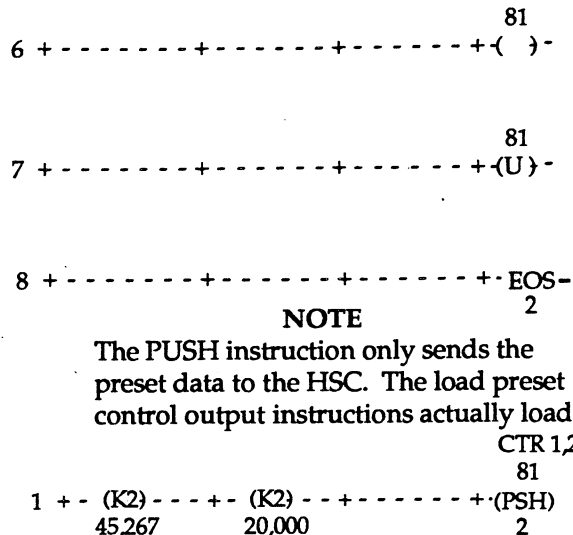
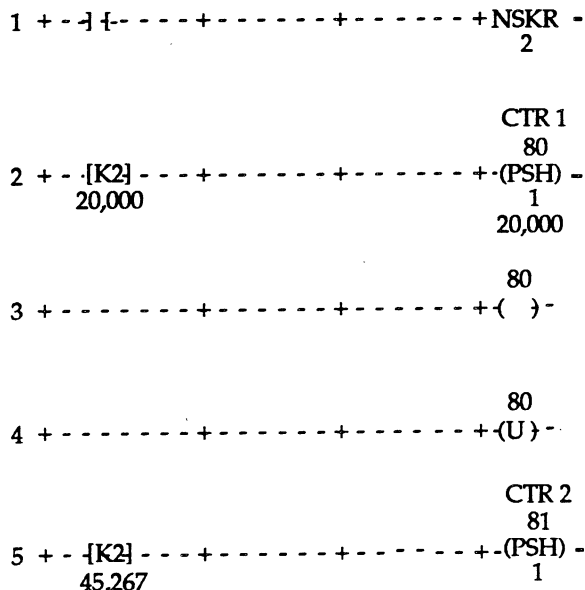
An installed HSC occupies two I/O card slots and assumes these card slots addresses. Each slot should be selected for 8-point operation.

When the HSC is installed in slots selected for 16-point operation, the HSC utilizes the eight least significant addresses of each slot.

The following programming explanation, assumes that the HSC is installed in two card slots that are addressed 80 through 95 (8-point operation).

The PUSH instruction is used to send the preset values to the HSC module. A PUSH to the least significant address (LSA) will send a preset value to counter #1. A PUSH to the LSA + 1 will send a preset value to counter #2. See the following logic. Turning address 80 on then unlatching it sends a pulse that allows the preset values to go to the counter.

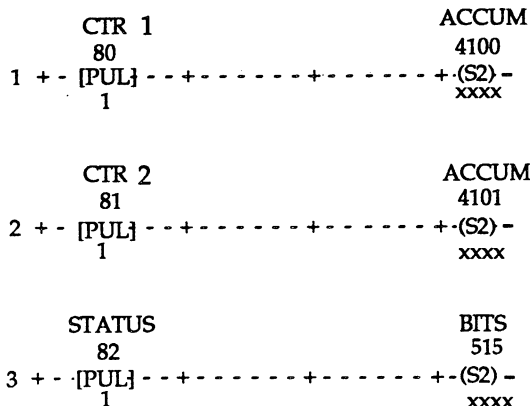
Both preset values may be sent to the HSC simultaneously by using a PUSH 2 instruction, as illustrated below.



The PULL instruction is used to obtain accumulated values and module status bit information.

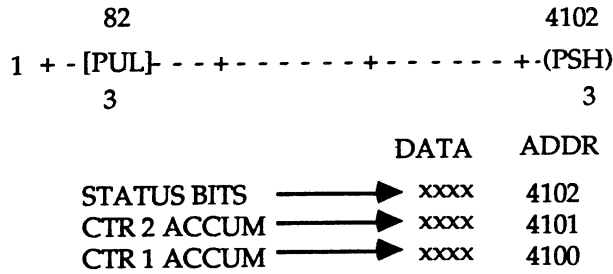
A PULL to the module's least significant address (LSA) will obtain the accumulated value for counter #1. A PULL from LSA + 1 will obtain counter #2 accumulated value. A PULL from LSA + 2 will obtain the status bit information. See the following logic.

A PULL 3 instruction from the LSA + 2 will obtain status bits and counter accumulated values simultaneously. See the following.



NOTE

The HSC accumulated values and status bits may be read numerous times in one processor program scan



by programming the PULL instruction as often as necessary throughout the control program.

HSC Status Bits

Module status information is contained in a single 16-bit register. See Figure 5. A PULL from the HSC LSA + 2 will obtain module status bit information.

The register contents may be examined by sending the status bit word to 16 consecutive control relay addresses through a SEND OUT instruction, as the logic below illustrates.

Count Direction (Bit 0): This bit indicates counter direction. When the bit is on, both 16-bit counters are counting down. When it is off, counters are incrementing.

Overflow Counter #1 (Bit 1): Bit 1 will turn on under the following conditions:

1. Counter is incrementing through 65,535.

2. Counter has decremented past zero and then reverses direction to increment beyond zero.

Both of these conditions will cause the overflow bit (flag) to turn on. This bit is latched and must be reset by user program control by using the clear counter flags control output.

Underflow Counter #1 (Bit 2): Bit 2 will turn on under the following conditions:

1. Counter is decrementing and decrements through zero.
2. Counter has incremented past 65,535 and then reverses direction to decrement through 65,535.

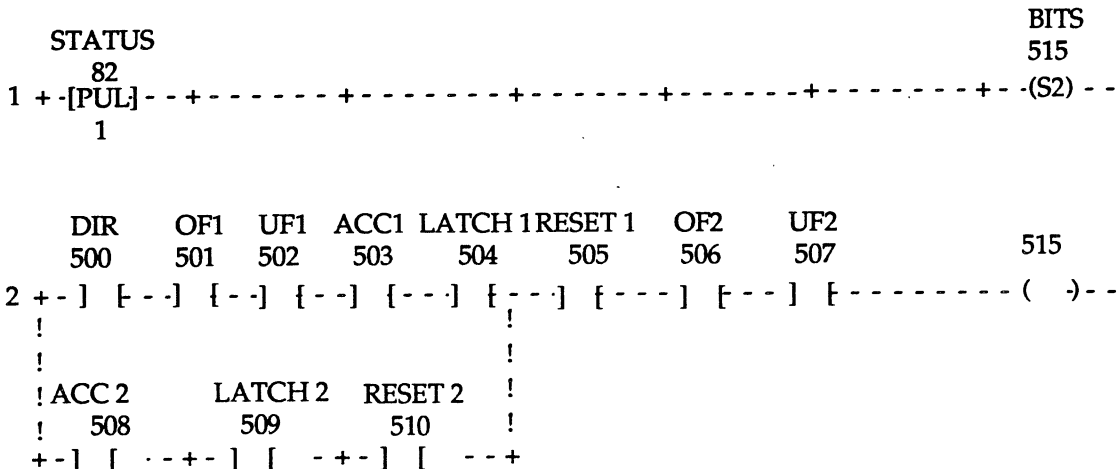
Both of these conditions will cause the underflow bit (flag) to turn on. This bit is latched and must be reset by the user program control by using the clear counter flag's control output.

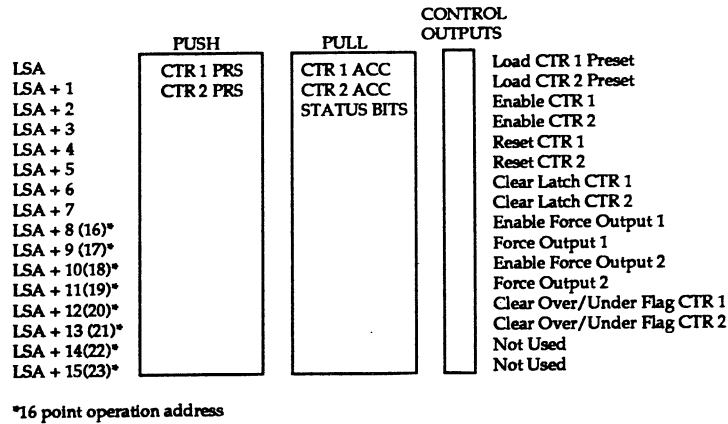
NOTE

The 16-bit counters, while incrementing through 65,535, will reset to zero and resume incrementing while turning on the overflow flags. The 16-bit counters, while decrementing through zero, will reset to 65,535 and resume decrementing while turning on the underflow flags.

Accumulated Count Greater Than or Equal to Preset Counter #1 (Bit 3): This bit will turn on when the accumulated value equals or exceeds the preset value. It will be off when these conditions are not true.

Latch Counter #1 (Bit 4): This status bit, when on, indicates that counter #1 has received an external latch input command and is in the latched state. This status bit is turned off when the counter is reset by either the external reset input, program rest control





STATUS BITS

0	Count Direction
1	Overflow Counter #1
2	Underflow Counter #1
3	Accumulated Count ≥ Preset Counter #1
4	Latch Counter #1
5	External Reset Counter #1
6	Overflow Counter #2
7	Underflow Counter #2
8	Accumulated Count ≥ Preset Counter #2
9	Latch Counter #2
10	External Reset Counter #2
11	Not Used
12	Not Used
13	Not Used
14	Not Used
15	Not Used

FIGURE 5 - HSC STATUS BITS

output, or the program clear latch counter #1 control output.

External RESET Counter #1 (Bit 5): This bit indicates the state of the external counter #1 reset input. When on, the reset input is energized. When off, the external reset input is de-energized.

Overflow Counter #2 (Bit 6): Same as Bit 1.

Underflow Counter #2 (Bit 7): Same as Bit 2.

Accumulated Counter Greater Than or Equal to Preset Counter #2 (Bit 8): Same as Bit 3.

Latch Counter #2 (Bit 9): Same as Bit 4.

External Reset #2 (Bit 10): Same as Bit 5.

Bits 11 through 15 are not used.

Control Output Operations

12 Control Output coils (-) that are programmed to

specific module addresses allow the user program to perform the following functions:

- Load preset values
- Enable/disable counters
- Reset counters
- Clear flag status bits
- Clear latch counter conditions
- Force HSC outputs on or off

The 16 control output addresses and their functions are listed below. (LSA = Least Significant HSC Module Address). Refer to Figure 5.

LSA =	Load Counter #1 Preset
LSA + 1 =	Load Counter #2 Preset
LSA + 2 =	Enable Counter #1
LSA + 3 =	Enable Counter #2
LSA + 4 =	Reset Counter #1
LSA + 5 =	Reset Counter #2
LSA + 6 =	Clear Latch Counter #1
LSA + 7 =	Clear Latch counter #2

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Industrial Automation and Control
Honeywell Inc.
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